Technical Specification for VME Interface Controller

Table of Contents

List of Figures

List of Tables

1 Introduction

1.1 Overview

The VMEbus specification defines an interfacing system used to interconnect data processing, data storage, and peripheral control devices in a closely coupled hardware configuration.

iWave Systems has introduced VME controller which can be implemented on FPGA. It supports the following features:

1.2 Features

- 16-bit VME controller
- Interface to Atmel ARM EBI interface
- Status indication LEDs
- Internal configuration registers for configuring the modes

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
BA	Base address
CPU	Central Processing unit
FPGA	Field Programmable Gate Array
NC	No connection
RAM	Random Access memory
GND	Ground
LED	Light Emitting Diode
VME	Versa Module Euro Card
AM	Address Modifier

2 System Level Block Diagram

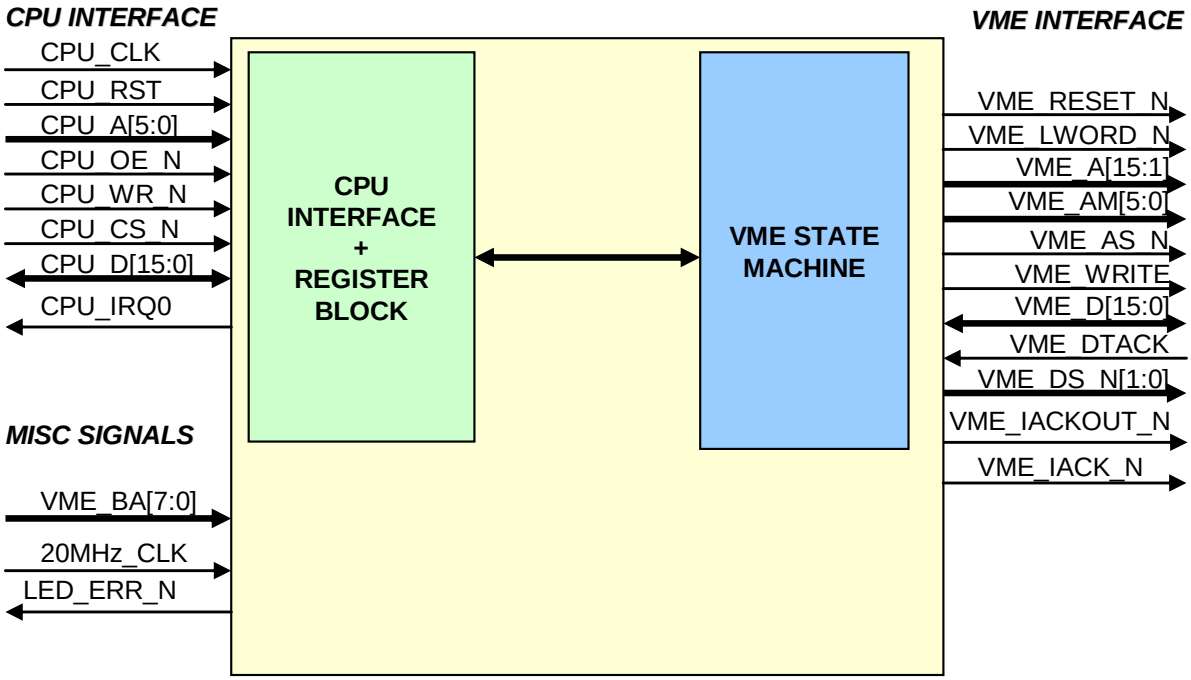

Figure 1: System Level Diagram

2.1 Processor Interface

This is the interface to the Atmel processor EBI bus. Asynchronous memory interface of the EBI can be used to access the internal registers of the FPGA. It can also access the VME slaves through the internal registers.

2.2 P1 Interface

This is the interface towards the VME bus. This interface acts as the VME Master and is controlled by the VME State Machine. The VME State Machine generates all the control signals towards the VME bus and takes care of the data transfer on the VME bus. Once the transaction is completed, it generates and interrupts to the processor to indicate the completion of the current bus cycle.

Only the following VME cycles are supported.

1. Basic Read/Write cycle - Only one chunk of data is transferred per cycle
2. IACK cycle - To support the Interrupts on the bus

Other cycles like Block Data transfer, Read-modify-write cycle, Address only cycle etc are not supported.

2.3 VME Interrupt logic

This block acts as the Interrupt controller of the system. Whenever there is an interrupt, this block handles the interrupt cycles and eventually interrupts the ATMEL processor. This block handles the IACK chain and the status/ID handling.

2.4 I/O Description

The I/O signals of the FPGA are described below.

2.4.1 Processor EBI Interface Signal Description

Table 2: Processor EBI Interface Signal Description

SIGNAL	I/O	No of Pins	DESCRIPTION
CPU_CLK	I	1	75MHz clock input from the ATMEL processor. All processor cycles are handled using this clock
CPU_RST	I	1	Asynchronous reset from processor
CPU_A[5:0]	I	6	Address bus
CPU_D[15:0]	I/O	16	Data bus
CPU_OE_N	I	1	Active low output enable 0 → Read from the processor 1 → No Read
CPU_WR_N	I	1	Active low Write enable 0 → Write from CPU 1 → No Write
CPU_CS_N	I	1	Chip enable Signal
CPU_IRQ0	O	1	Interrupt to the CPU to indicate that the read or write cycle to VME is completed

2.4.2 P1 Connector (VME Interface) Signal Description

Table 3: P1 Connector (VME Interface) Signal Description

SIGNAL	I/O	No of Pins	DESCRIPTION
VME_RESET_N	O	1	Active low reset to the VME bus
VME_A[15:0]	O	16	Address output to the slaves
VME_AM[5:0]	O	6	These are used to indicate the slave the type of data transfer the master is dealing with the slave
VME_DS_N[1:0]	O	2	Active low output signals indicate the valid data on the data bus. These signals serve not only to qualify data, but also to indicate the size and position of the data transfer.
VME_LWORD_N	O	1	Driven along with other signals during data transfer signals to indicate that the current cycle is a 32-bit cycle. LWORD is permanently pulled high in this design.
VME_D[15:0]	I/O	16	VME data bus. Only 16-bit data transactions are supported.
VME_AS	O	1	Address strobe signal to indicate that the valid address on the address bus
VME_DTACK	I	1	Slave drives this signal to indicate a successful write transaction. During read transactions, this indicates valid data on the data bus.
VME_WRITE	O	1	Used to indicate the direction of the data transfer 0→Direction of transfer is from master to slave 1→Direction of transfer is from slave to master
VME_IACKOUT_N	O	1	Used to drive daisy chain driver, fixed to VCC
VME_IACK_N	O	1	It is used to acknowledge the interrupter, fixed to VCC

2.4.3 Miscellaneous Signal Description

Table 4: Miscellaneous Signal Description

SIGNAL	I/O	No of Pins	DESCRIPTION
VME_BA[7:0]	I	8	These signals are inputs form a DIP switch on the board. These 8 bits define the base address of the 512 bytes control space on the VME bus. These bits define the MSB 8 bits of the control space.
LED_ERR_N	O	1	Turns on, when an error occurs, turns off the lights when Processor clear that
CLK_20MHZ	I	1	20MHz clock input for P1 interface

3 Register Details

3.1 Register List

Table 5: Register List

Sl. No	Register Name	Width	Read/ Write	Address[5:0]
1.	VME Address Modifier And Control Register	16	R/W	0x00
2.	VME Data Register	16	R/W	0x04
3.	VME Address Register	16	R/W	0x08
4.	General Purpose Register	16	R/W	0x0C
5.	VME Bus Error Timer	16	R/W	0x10
6.	VME Base Address Register	16	R	0x14
7.	VME Interrupt Status Register	16	R	0x18
8.	VME Interrupt Enable Register	16	R/W	0x1C
9.	LED Control Register	16	R/W	0x34

3.2 Register Description:

3.2.1 VME Address Modifier And Control Register

Table 6: VME Address Modifier And Control Register

VME Address Modifiers & Control Registers		**Address offset: [5:0] = 0X00**		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:10	Reserved	R	0	These bits are reserved for future use
9:8	DS[1:0]	R/W	0	These bits are transmitted as data strobe value during VME cycles. Processor should configure these bits depending on the bus width of the current cycle. 00→ Double byte transfer 01→ Even Single byte transfer 10→ Odd Single byte transfer
7	WRITE	R/W	0	This bit is used to indicate that the processor wants to write the data to the slave through the VME Bus. This bit is automatically cleared as soon as the write cycle is completed. 0 → No Write 1 → Write to the Slave
6	READ	R/W	0	This bit is used to indicate that the processor wants to read the data from the slave through the VME Bus. This bit is automatically cleared as soon as the write cycle is completed. 0 → No Read 1 → Read from the Slave
5:0	AM[5:0]	R/W	0	This is used to pass additional binary information to the slave during data transfer cycle 111111→Standard supervisory block transfer 111110→ Standard supervisory program access 111101→ Standard supervisory data access 111011→Standard non privileged block transfer 111010→ Standard non privileged program access

VME Address Modifiers & Control Registers		Address offset: [5:0] = 0X00		
				111001→ Standard non privileged data access 101101→Short Supervisory access 101001→Short Non privileged access 001111→Extended supervisory block transfer 001110→Extended supervisory program access 001101→ Extended supervisory data access 001011→Extended non privileged block transfer 001010→ Extended non privileged program access 001001→ Extended non privileged data access *remaining all are reserved

3.2.2 VME Data Register

This register is used to store the data to be transferred to / from VME slaves.

Table 7: VME Data Register

VME Data Registers		Address offset: [5:0] = 0X04		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:0	DATA	R/W	0	During write cycles towards the VME bus, data to be written should be stored in this register before Write command id given. During read cycles, data read from VME slave is stored in this register for processor access.

3.2.3 VME Address Register

Table 8: VME Address Register

VME Address Registers		Address offset: [5:0] = 0X08		
Bit	**Bit name**	**R/W**	**Default**	**Description**

VME Address Registers		Address offset: [5:0] = 0X08		
15:0	ADDR	R/W	0	Processor has to store the address to be applied on the VME bus in this register before configuring Read/Write command ADDR[01] should be considered depending on the byte being accessed. ADDR[15:1] → 15-bit VME address bus ADDR[0] → Reserved

3.2.4 General Purpose Register

Table 9: General Purpose Register

General Purpose Register		Address offset: [5:0] = 0X0C		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:0	GPR	R/W	0	This is a 16-bit general purpose register. CPU can write/read this register for testing purposes.

3.2.5 VME Bus Error Timer

Table 10: VME Bus Error Timer

VME Bus Error Timer		Address offset: [5:0] = 0X10		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:0	BusErrTimer	R/W	0x00C8	This field defines the value of the counter used to generate timeout during cycles on the VME bus. The 20MHz internal clock is divided internally with this value. The default value generates a time out of 10us.

3.2.6 VME Base Address Register

Table 11: VME Base Address Register

VME Base Address Register		**Address offset: [5:0] = 0X14**		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:8	Reserved	R	0	These bits are reserved for future use
7:0	VME Base Address	R	XX	This register reflects the 8 bit base address input from the DIP switch. Processor should read this register to find the base address of the VME control space

3.2.7 VME Interrupt Status Register

These are used to indicate the status of the interrupts to the CPU generated either by the FPGA or by the slave.

Table 12: VME Interrupt Status Register

VME Interrupt Status Register		**Address offset: [5:0] = 0X18**		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:10	Reserved	-	0x00	Reserved.
9	BusErr	R	0	This bit is used to indicate that the error has occurred in the data transaction between the Master and the slave during the previous cycle 1 → Bus Error has occurred 0 → No Bus Error This interrupt is cleared automatically when the processor reads this register

VME Interrupt Status Register		**Address offset: [5:0] = 0X18**		
8	Read Done	R	0	This bit is used to indicate the status of the interrupt that is generated when reading the data from the slave is completed. 1 → VME slave read completed successfully 0 → VME slave read is not yet complete This interrupt is cleared automatically when the processor reads this register
7	Write Done	R	0	This bit is used to indicate the status of the interrupt that is generated when writing the data to the slave is completed. 1 → VME slave write completed successfully 0 → VME slave write is not yet complete This interrupt is cleared automatically when the processor reads this register
6:0	Reserved	R	0	Reserved

3.2.8 VME Interrupt Enable Register

These are used to enable the interrupts to the CPU generated by either the FPGA or the slave.

Table 13: VME Interrupt Enable Register

VME Interrupt Enable Register		**Address offset: [5:0] = 0X1C**		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:10	Reserved	R	0x00	These bits are reserved for future use
9	BusErr IE	R/W	0	This bit if set masks the interrupt generated buy Bus Error 1 → Bus Error interrupt is enabled 0 → Bus Error interrupt is disabled

VME Interrupt Enable Register		Address offset: [5:0] = 0X1C		
8	Read Done IE	R/W	0	This bit is used to enable / disable the Read Done interrupt 1 → Read Interrupt Enabled 0 → Read Interrupt Disabled
7	Write Done IE	R/W	0	This bit is used to enable / disable the Write Done interrupt 1 → Write Interrupt Enabled 0 → Write Interrupt Disabled
6:0	Reserved	R	0	These bits are reserved for future use

3.2.9 LED Control Register

Table 14: LED Control Register

LED Control Register		Address offset: [5:0] = 0X34		
Bit	**Bit name**	**R/W**	**Default**	**Description**
15:2	Reserved	R	0	These bits are reserved for future use
0	LED_ERR	R/W	0	This bit is used to glow the error LED of the Status LEDs 0→ Will not glow 1→ Will glow

4 Waveforms

4.1 P1 VME Write Cycle

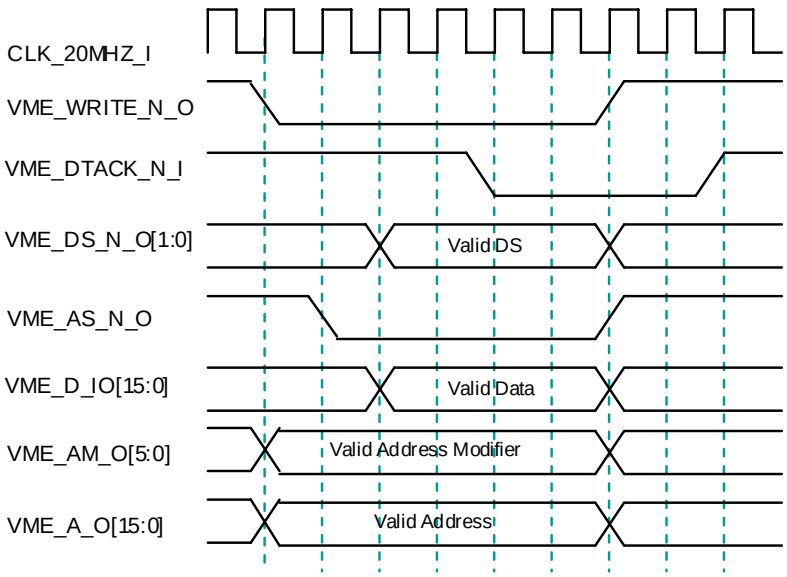

Figure 2: VME Address & Data Transaction waveform

4.2 P1 VME Read Cycle

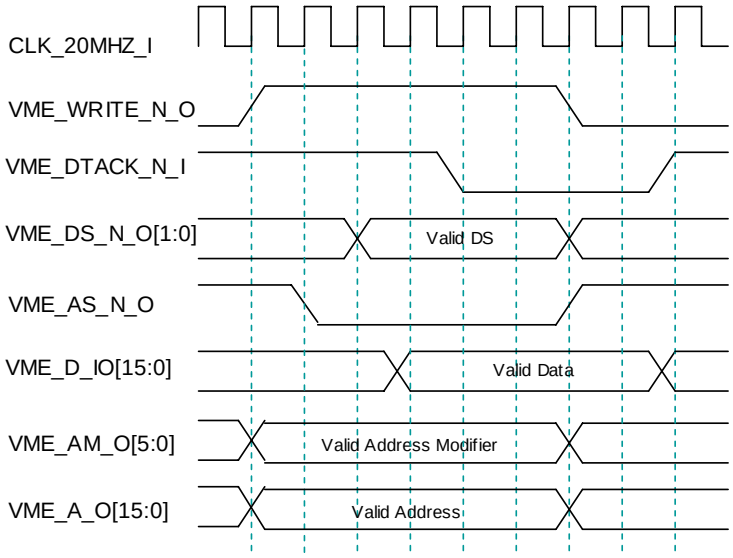

Figure 3: VME Address & Data Transaction waveform

4.3 Processor Write Cycle:

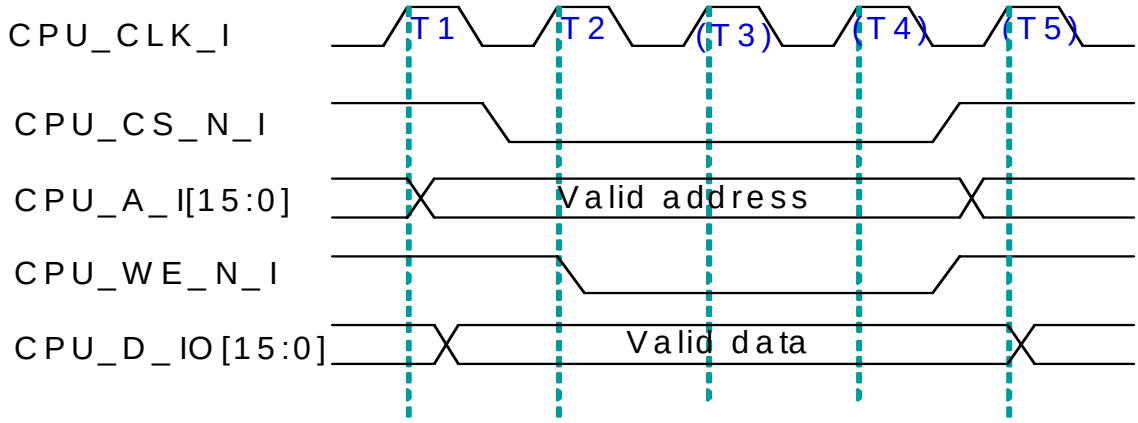

Figure 4: Processor Write Cycle

4.4 Processor Read Cycle:

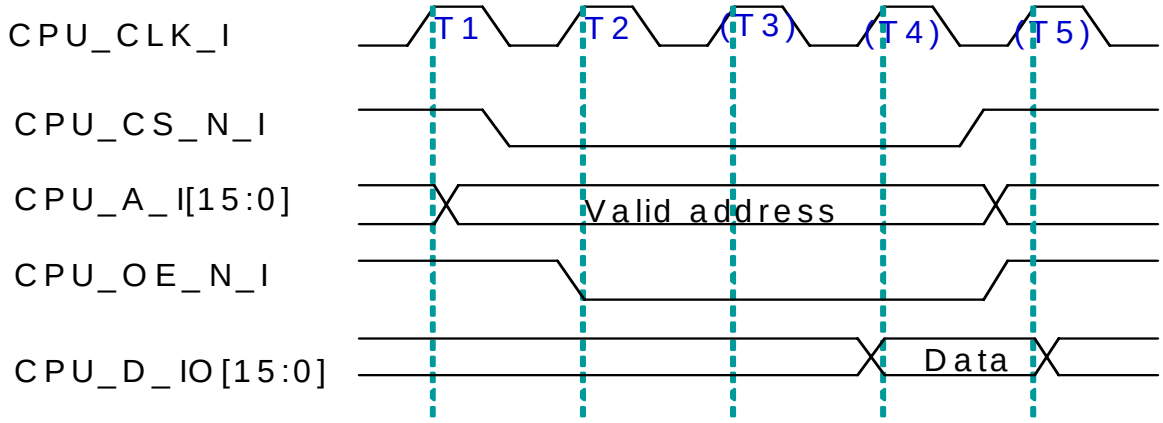

Figure 5: Processor Read Cycle